QIA128/IDC150/IEM100

SPI Communication Guide

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General Description

The QIA128/IDC150/IEM100 is a single-channel, ultra-low-power digital controller featuring UART and SPI interfaces.

Pin Configurations and Function Descriptions

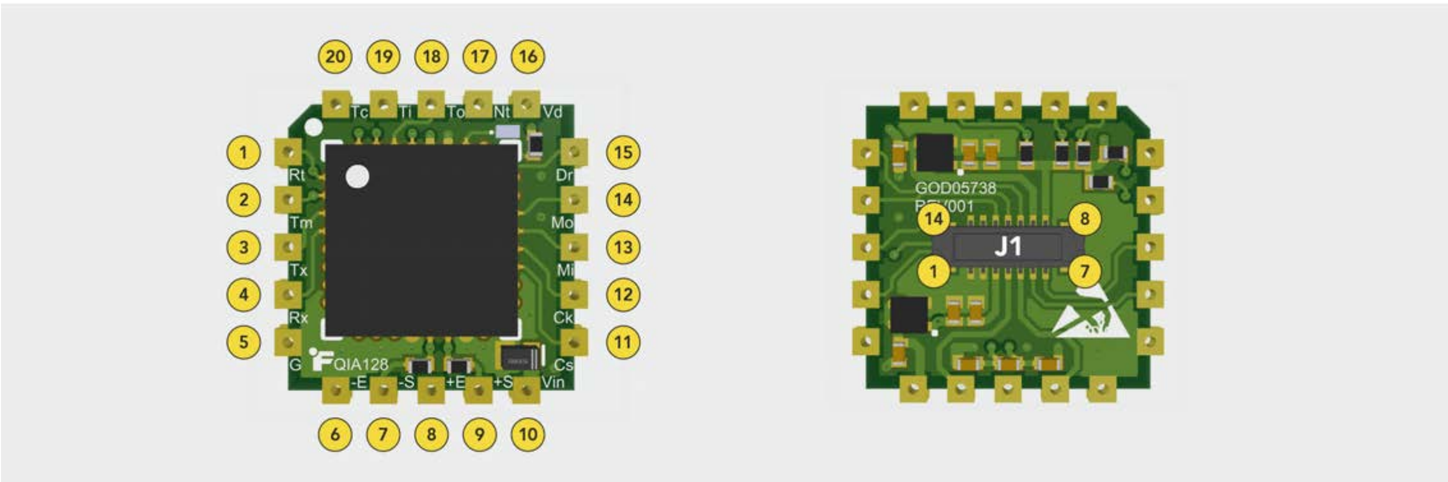

Figure 1.

TABLE 1			
#	**PIN**	**DESCRIPTION**	**J1#**
1	$\overline{RESET}$	Active low reset input.	-
2	TMS	JTAG Test Mode Select input for debug and firmware download.	-
3	RX	UART receive data input.	7
4	TX	UART transmit data output.	6
5	GND	Ground. All ground pins are internally connected.	1
6	–Excitation	Sensor excitation return, internally connected to GND.	2
7	–Signal	Sensor negative input.	5
8	+Excitation	Sensor excitation output.	3
9	+Signal	Sensor positive input.	4
10	VIN	Supply input, 3 to 5 VDC.	9
11	$\overline{CS}$	Active low chip select input. Do not assert $\overline{CS}$ low until the device has completed boot. Do not assert $\overline{CS}$ low unless $\overline{DRDY}$ is low.	14
12	SCLK	SPI serial clock input from host.	13

TABLE 1			
#	**PIN**	**DESCRIPTION**	**J1#**
13	HICO	SPI Host In Client Out data line.	12
14	HOCI	SPI Host Out Client In data line.	11
15	$\overline{DRDY}$	Active low data ready output. Indicates new sampled data is available and keeps host communication synchronized. $\overline{DRDY}$ goes low when data is ready to be clocked out and may be used as a host interrupt. $\overline{DRDY}$ is high during conversion and returns low when new data is available. **Note:** $\overline{DRDY}$ does not return high after data is read. It returns high only when the system enters a conversion state.	10
16	VDD	Digital supply rail, 2.5 V.	-
17	NTRST	JTAG NTRST and boot mode control input for debug and firmware download only.	-
18	TDO	JTAG Test Data Out.	-
19	TDI	JTAG Test Data In.	-
20	TCK	JTAG test clock input for debug and firmware download.	-

QIA128/IDC150/IEM100 SPI Configuration

TABLE 2	
Serial Word Length	8-Bit
SPI Mode	Mode 0 (CPOL = 0, CPHA = 0)
SCLK Frequency	Min: 1 MHz, Max: 2 MHz
Internal Clock Frequency of MCU	10.24 MHz
Operation Mode	Client
Voltage Level	1.8 VDC (compatible with 3.3 VDC)

Note:

- The units have been tested with SCLK of 2MHz.
- The QIA128/IDC150/IEM100 (client device) operates on a 1.8 VDC logic level and is compatible with logic levels up to 3.3 VDC, allowing for direct connection. If the host device's input threshold for logic high (VIH) supports 1.8 VDC, no additional hardware or considerations are required. Otherwise, a level shifter may be necessary to ensure proper communication.

$\overline{DRDY}$ Pin Functionality

When the $\overline{DRDY}$ pin is high, the device is performing data conversion and post-processing. $\overline{DRDY}$ transitions low immediately once the conversion and associated post-processing are complete.

Note: *The $\overline{DRDY}$ signal can be used at the system level to synchronize data transfer and timing between the host and the device, when required.*

$\overline{DRDY}$ Period:

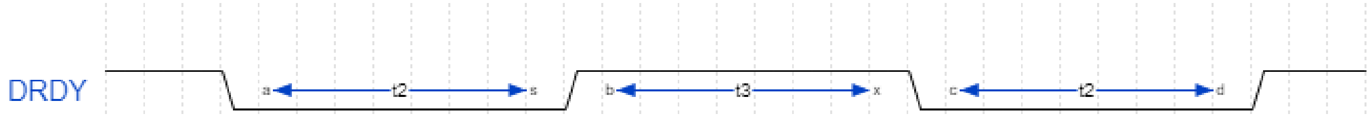

Figure 2.

The following table shows the high and low timing periods of the $\overline{DRDY}$ signal for all supported sampling rates.

TABLE 3

t_2 (ms)	t_3 (µs)	DESCRIPTION
240	125	4 SPS
55		20 SPS
19		50 SPS
9		100 SPS
4.5		200 SPS
1.5		500 SPS
1.1		850 SPS
0.6		1300 SPS

Continuous Read Mode

The ***GADC*** command can be issued during each $\overline{DRDY}$ period to continuously retrieve ADC data.

Note: *If either the CRC or CMD byte is invalid, the device will still populate the buffer with the ADC data followed by the CRC8 value.*

SPI Packet Structure

he packet structure remains consistent across all transactions and always consists of four data bytes for both transmitted and received data.

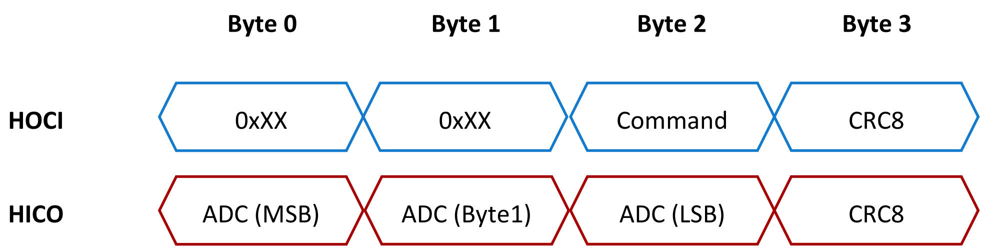

Figure 3.

Timing Diagrams

Packet Structure

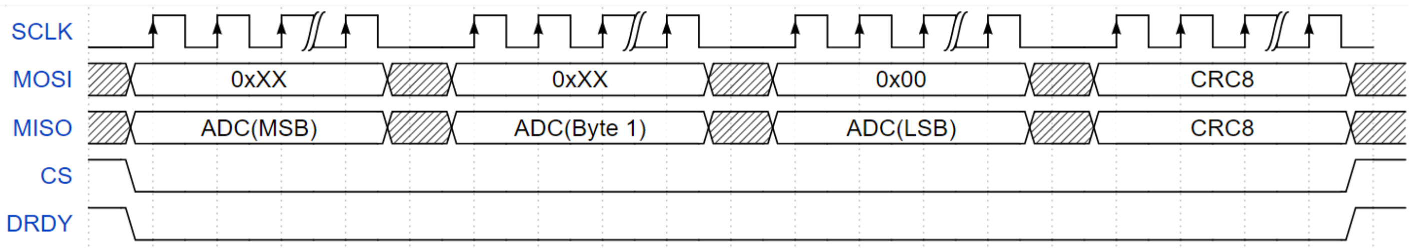

Figure 4.

Notes:

- In Figure 4, each clock corresponds to 8 bits.
- Each word (8-bit) may be clocked out with or without delay, provided that the full transaction is completed within a single $\overline{DRDY}$ period.

System Behavior

Start-up and Self-Calibration Mode

At power-up, the device reads configuration data from internal flash memory and then enters internal self-calibration.

Note: *The first* $\overline{DRDY}$ *pulse can be used as an indication that the device has completed initialization and is ready for system-level communication.*

Sampling Rate Change

When a sampling rate change is requested, the updated $\overline{DRDY}$ period will be reflected within 0.5 seconds, depending on the selected sampling rate.

Sampling Rates

TABLE 4

Maximum Approximate data rate change timing (ms)	SR Code	Sampling Rate
≅250	0x00	4 SPS
	0x01	20 SPS
	0x02	50 SPS
	0x03	100 SPS
	0x04	200 SPS
	0x05	500 SPS
	0x06	850 SPS
	0x07	1300 SPS

Command-Set List

TABLE 5										
			HOCI Line Packet Structure (Host to QIA128/IDC150/IEM100)				HICO Line Packet Structure (QIA128/IDC150/IEM100 to Host)			
					CMD	CRC	Payload	Payload	Payload	CRC
#	NAME	DESCRIPTION	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 0	BYTE 1	BYTE 2	BYTE 3
Get	GADC	Get ADC Data	0xXX	0xXX	0x00	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP0	Get Calibration Point Zero	0xXX	0xXX	0x01	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP1	Get Calibration Point One	0xXX	0xXX	0x02	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP2	Get Calibration Point Two	0xXX	0xXX	0x03	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP3	Get Calibration Point Three	0xXX	0xXX	0x04	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP4	Get Calibration Point Four	0xXX	0xXX	0x05	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP5	Get Calibration Point Five	0xXX	0xXX	0x06	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP6	Get Calibration Point Six	0xXX	0xXX	0x07	CRC8	ADC MSB	ADC Byte 1	ADC LSB	CRC8
Get	GCP7	Get Calibration Point Seven	0xXX	0xXX	0x08	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP8	Get Calibration Point Eight	0xXX	0xXX	0x09	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP9	Get Calibration Point Nine	0xXX	0xXX	0x0A	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP10	Get Calibration Point Ten	0xXX	0xXX	0x0B	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP11	Get Calibration Point Eleven	0xXX	0xXX	0x0C	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP12	Get Calibration Point Twelve	0xXX	0xXX	0x0D	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP13	Get Calibration Point Thirteen	0xXX	0xXX	0x0E	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP14	Get Calibration Point Fourteen	0xXX	0xXX	0x0F	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP15	Get Calibration Point Fifteen	0xXX	0xXX	0x10	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP16	Get Calibration Point Sixteen	0xXX	0xXX	0x11	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP17	Get Calibration Point Seventeen	0xXX	0xXX	0x12	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP18	Get Calibration Point Eighteen	0xXX	0xXX	0x13	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP19	Get Calibration Point Nineteen	0xXX	0xXX	0x14	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP20	Get Calibration Point Twenty	0xXX	0xXX	0x15	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP21	Get Calibration Point Twenty-One	0xXX	0xXX	0x16	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GCP22	Get Calibration Point Twenty-Two	0xXX	0xXX	0x17	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8
Get	GSSN	Get Sensor Serial Number	0xXX	0xXX	0x18	CRC8	SSN MSB	SSN Byte1	SSN LSB	CRC8
Get	GISN	Get Instrument Serial Number	0xXX	0xXX	0x19	CRC8	ISN MSB	ISN Byte1	ISN LSB	CRC8
Get	GFRN	Get Firmware Revision Number	0xXX	0xXX	0x1A	CRC8	Major	Minor	Patch	CRC8

TABLE 5

			HOCI Line Packet Structure (Host to QIA128/IDC150/IEM100)				HICO Line Packet Structure (QIA128/IDC150/IEM100 to Host)			
					CMD	CRC	Payload	Payload	Payload	CRC
#	NAME	DESCRIPTION	BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 0	BYTE 1	BYTE 2	BYTE 3
Get	GDR	Get Data Rate	0xXX	0xXX	0x1B	CRC8	0x00	0x00	SR Code (See Tbl 4.)	CRC8
Set	S4SPS	Set 4 Sample Per Second	0xXX	0xXX	0x1C	CRC8	0x00	0x00	0x00	CRC8
Set	S20SPS	Set 20 Sample Per Second	0xXX	0xXX	0x1D	CRC8	0x00	0x00	0x00	CRC8
Set	S50SPS	Set 50 Sample Per Second	0xXX	0xXX	0x1E	CRC8	0x00	0x00	0x00	CRC8
Set	S100SPS	Set 100 Sample Per Second	0xXX	0xXX	0x1F	CRC8	0x00	0x00	0x00	CRC8
Set	S200SPS	Set 200 Sample Per Second	0xXX	0xXX	0x20	CRC8	0x00	0x00	0x00	CRC8
Set	S500SPS	Set 500 Sample Per Second	0xXX	0xXX	0x21	CRC8	0x00	0x00	0x00	CRC8
Set	S850SPS	Set 850 Sample Per Second	0xXX	0xXX	0x22	CRC8	0x00	0x00	0x00	CRC8
Set	S1300SPS	Set 1300 Sample Per Second	0xXX	0xXX	0x23	CRC8	0x00	0x00	0x00	CRC8
Get	GND	Get Number of Directions	0xXX	0xXX	0x27	CRC8	0x00	0x00	GND	CRC8
Get	GNLP	Get Number of Loading Points	0xXX	0xXX	0x28	CRC8	0x00	0x00	GNLP	CRC8
Get	GBT	Get Board Temperature	0xXX	0xXX	0x26	CRC8	ADC MSB	ADC Byte1	ADC LSB	CRC8

Notes:

- 0xXX = Don't care
- All pre-defined responses from each command that is sent on the HOCI line should be expected in the next $\overline{\text{DRDY}}$ period.

Payload Example

The following transaction shows the response to the GSSN command (Get Sensor Serial Number) being clocked out during the GADC command (Get ADC Data) transaction.

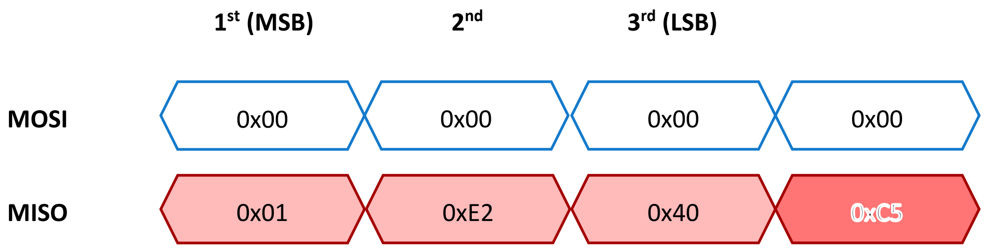

Figure 5.

Hex to decimal: 01E240 → 123456

Calibration Point Payload Example

The received packet payload follows the format defined in the Payload Example section above. Up to 11 calibration points are supported per direction. Point indexing is defined as follows:

- Point 0 is the positive direction offset.
- If the number of calibration points per direction is P
    - then the positive full-scale point is Point N, where N = P - 1.
    - The negative direction offset is Point N + 1.
    - The negative full-scale point is Point M, where M = (2 x P) - 1.

Example for a 2-point calibration:

- Point 0 = positive offset
- Point 1 = positive full-scale
- Point 2 = negative offset
- Point 3 = negative full-scale
- For this example, P = 2, therefore N = 1 and M = 3.

Example for a 5-point calibration:

- Point 0 = positive offset
- Point 4 = positive full-scale
- Point 5 = negative offset
- Point 9 = negative full-scale
- For this example, P = 5, therefore N = 4 and M = 9.

ADC Data Conversion

The following formula could be used to convert the raw ADC data:

$$CalculatedReading = \frac{[ADCValue - OffsetValue]}{[FullScaleValue - OffsetValue]} \times FullScaleLoad$$

The following variables are used in the ADC data conversion:

- **ADCValue** represents the most recent analog to digital conversion result.
- **OffsetValue** represents the analog to digital conversion value captured during calibration that corresponds to the offset condition, or zero applied physical load.
- **FullScaleValue** represents the analog to digital conversion value captured during calibration that corresponds to the full-scale condition, or maximum applied physical load.
- **FullScaleLoad** represents the calibrated numeric value corresponding to the maximum physical load. **Note:** Full scale load value can be found on the calibration certificate.

ADC Data Conversion Examples (Direction 1, 2-point Calibration)

Get calibration point 0 (Direction 1) *[GCP0]:*
Hex to decimal: `0x81B320` → `8,500,000`

Get calibration point 1 (Direction 1) *[GCP1]:*
Hex to decimal: `0xB71B00` → `12,000,000`

Get channel current reading *(GADC):*
Hex to decimal: `0x989680` → `10,000,000`

Calculation:

- **OffsetValue** = Get Calibration Point Zero (GCP0): `8,500,000`
- **FullScaleValue** = Get Calibration Point Five (GCP5): `12,000,000`
- **FullScaleLoad** = `20g` (Accessible via the calibration certificate or directly from onboard flash memory)

$$CalculatedReading = \frac{[10000000 - 8500000]}{[12000000 - 8500000\,]} \times 20g = 8.5714g$$

Temperature Conversion

$$Output\ (mV)\ =\ 1200 - [\frac{16777215\ - ADCValue}{6990.506666666667}]$$

$$Temperature\ (°C) =\ -40 + \left[\frac{Output - 80}{0.28}\right]$$

Temperature Conversion Example

ADCValue: Get Board Temperature (GBT): `9,095,859 (0x8ACAB3)`

$$1200 - \left[\frac{16777215\ - 9095859}{6990.506666666667}\right] =\ 101.1733\ (mV)$$

$$-40 +\ \left[\frac{101.1733\ - 80}{0.28}\right] =\ 35.6\ (°C)$$

Firmware Revision

QIA128	
Revision	7.0.0
Release Date	09/19/2023
Hardware Compatibility	REV002
Notes	**New Features** • Added support for hardware revision HW002 **Changes** • N/A **Fixes** • • N/A

IDC150/IEM100	
Revision	1.0.0
Release Date	04/10/2026
Hardware Compatibility	REV003
Notes	**New Features** • N/A **Changes** • The model number has been changed from IDC150 to IEM100. The firmware and hardware item numbers remain unchanged **Fixes** • N/A

CRC Calculations and References

The CRC8 calculation is implemented based on the reference repository listed below.
https://github.com/futekast/CRC8